

FIG. 1

FIG. 2A is a block diagram of a network architecture. The architecture includes a plurality of network processors (202, 204, 206, ..., 208), a plurality of virtual queue managers (VQM) (208, 210, 212, ..., 214), and a plurality of control switch units (CSW) (216, 218, 220, ..., 222). Each network processor (202, 204, 206, ..., 208) is connected to a corresponding VQM (208, 210, 212, ..., 214) via a bidirectional connection (220, 222, 224, ..., 226). Each VQM (208, 210, 212, ..., 214) is connected to a corresponding CSW (216, 218, 220, ..., 222) via a bidirectional connection (228, 230, 232, ..., 234). The network processors (202, 204, 206, ..., 208) are also connected to each other via a network (236). The VQM (208, 210, 212, ..., 214) are also connected to each other via a network (238). The CSW (216, 218, 220, ..., 222) are also connected to each other via a network (240).

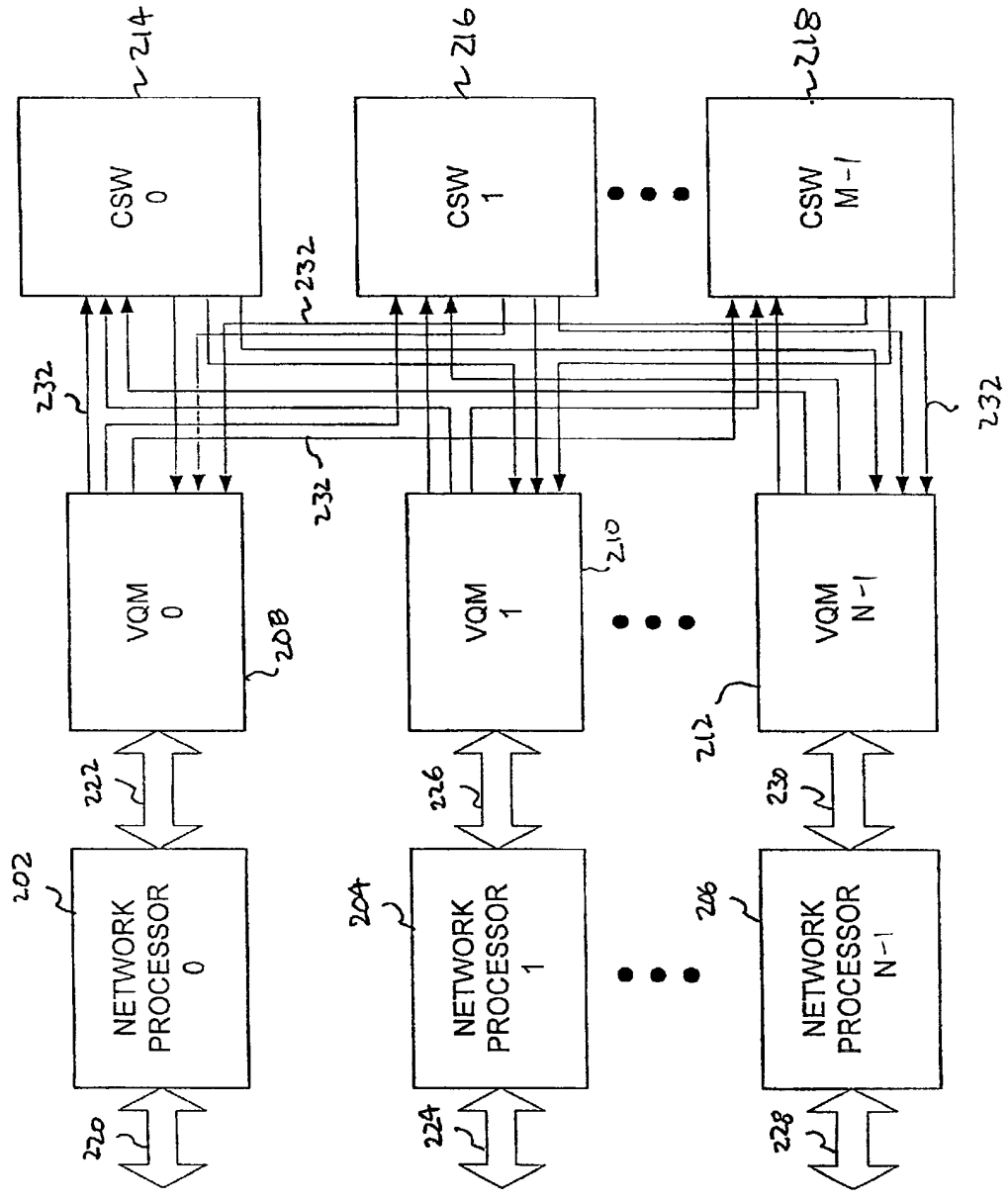


FIG. 2A

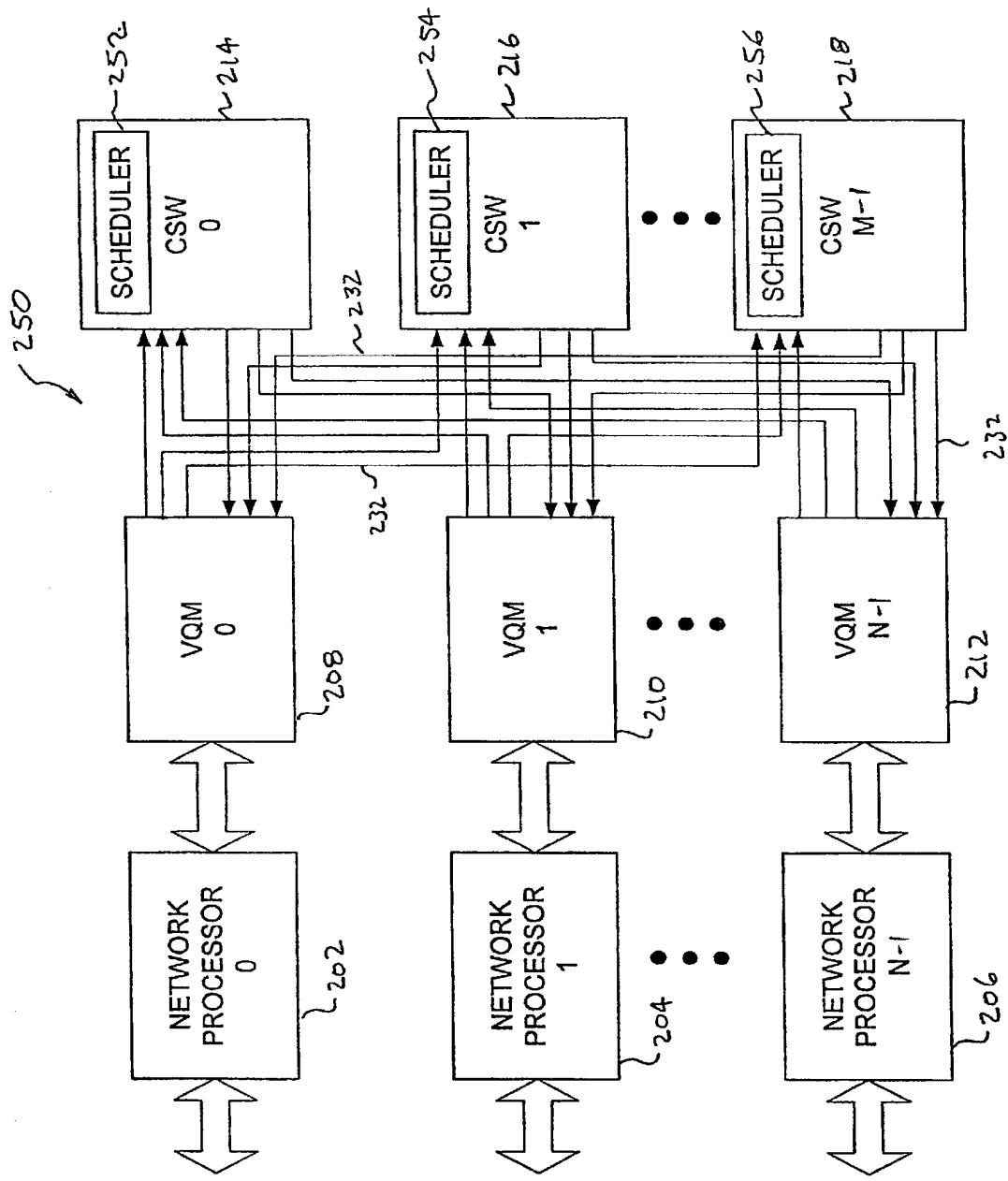


FIG. 2B

FIG. 2C is a block diagram of a network architecture 260. The architecture includes a plurality of network processors (202, 204, 206), a plurality of virtual queue managers (VQM) (208, 210, 212), a plurality of control state word (CSW) blocks (214, 216, 218), and a scheduler (262). The network processors are connected to the VQM blocks via bidirectional arrows. The VQM blocks are connected to the CSW blocks via bidirectional arrows. The CSW blocks are connected to the scheduler via bidirectional arrows. The scheduler is connected to the network processors via bidirectional arrows.

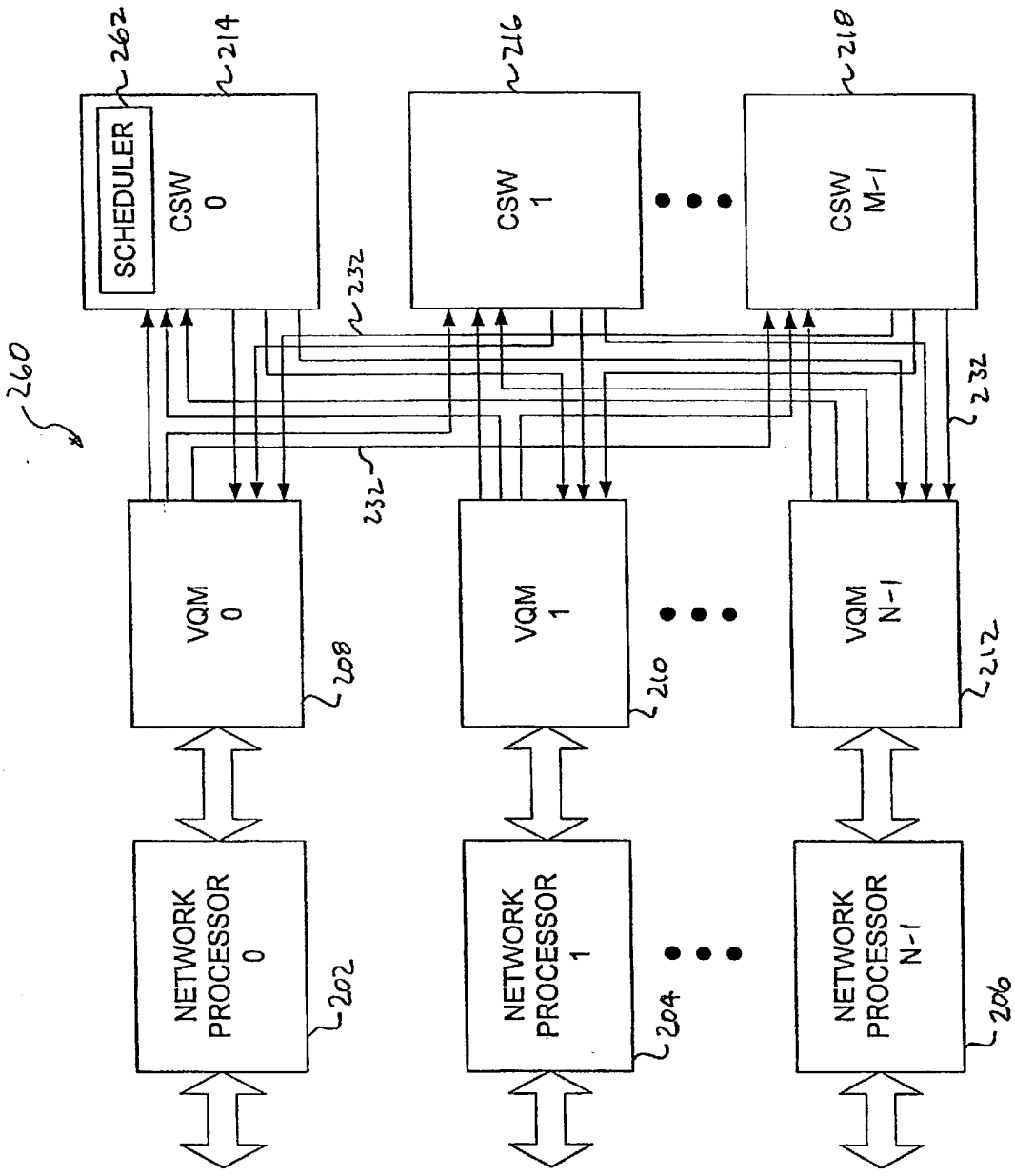


FIG. 2C

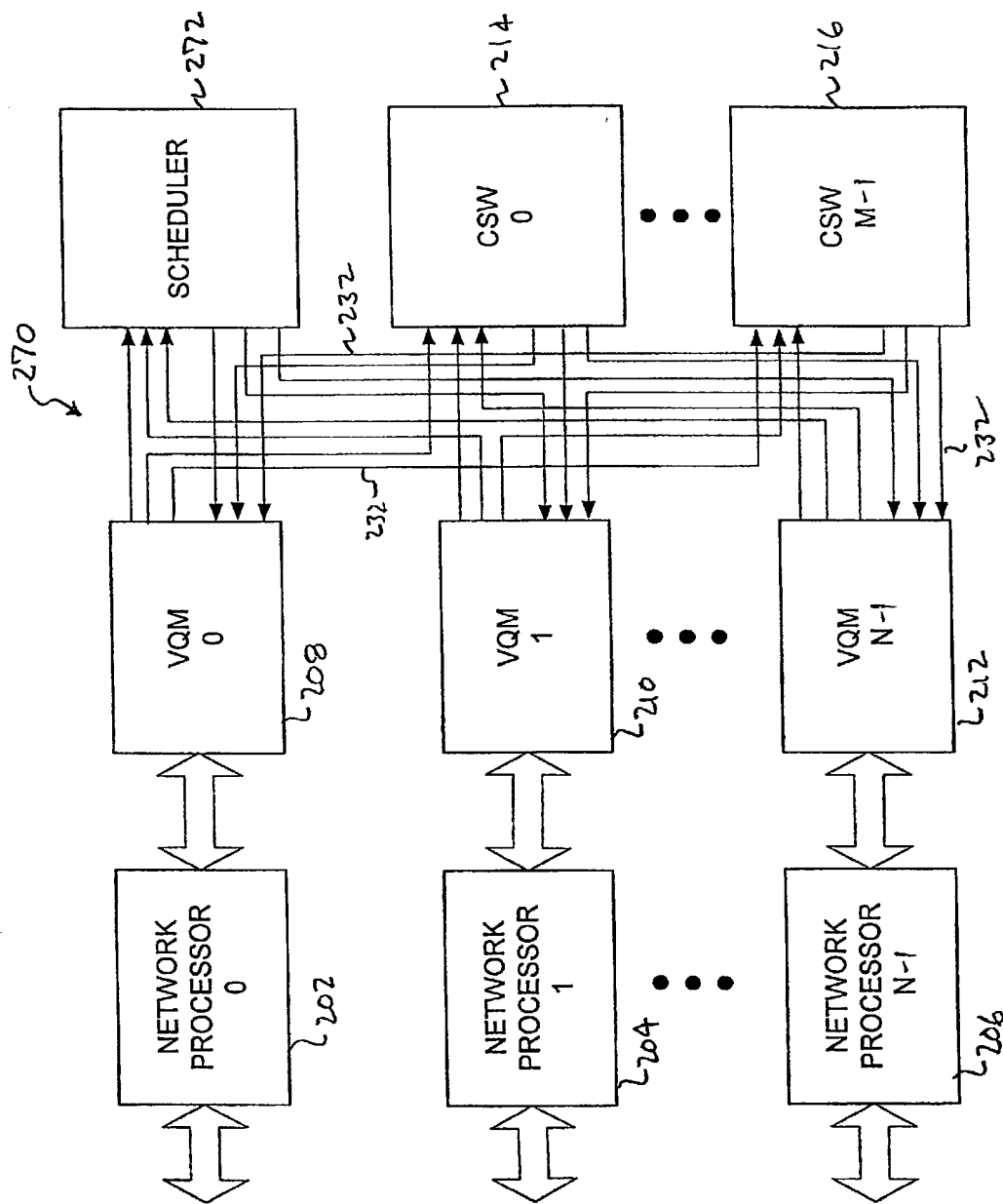


FIG. 2D

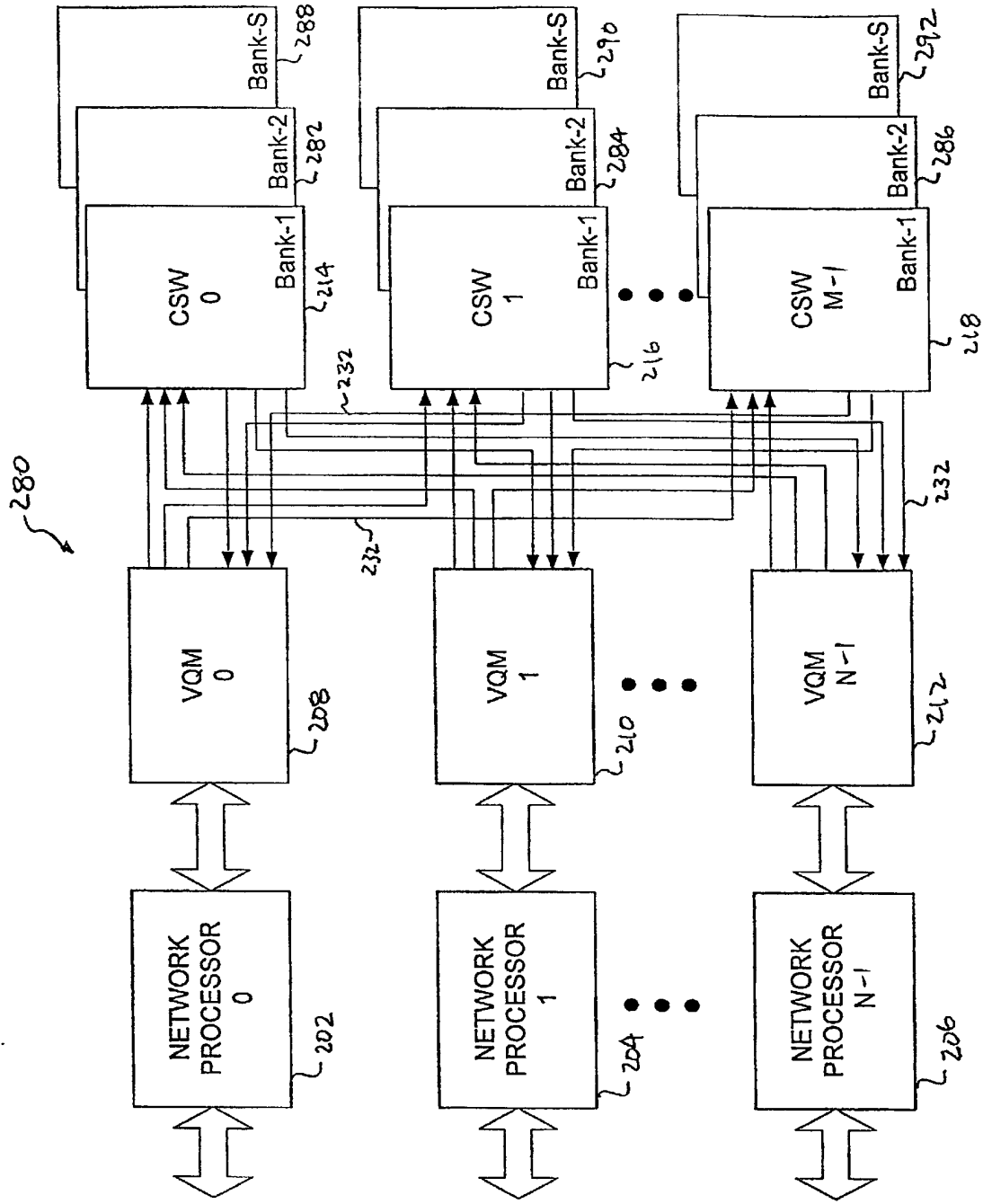


FIG. 2E

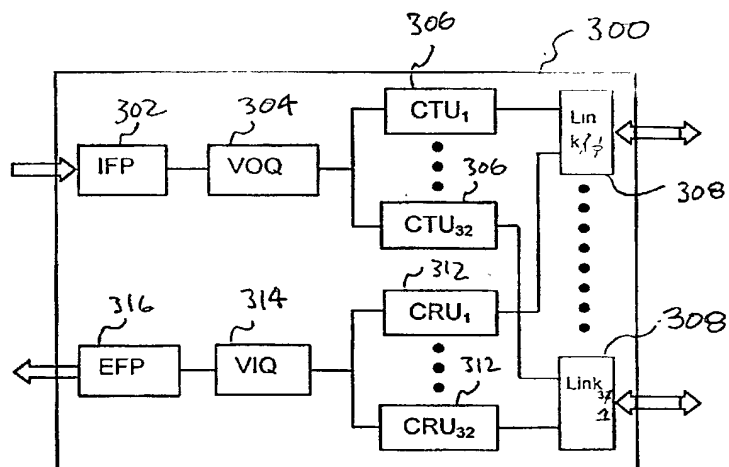


FIG. 3 [VQM]

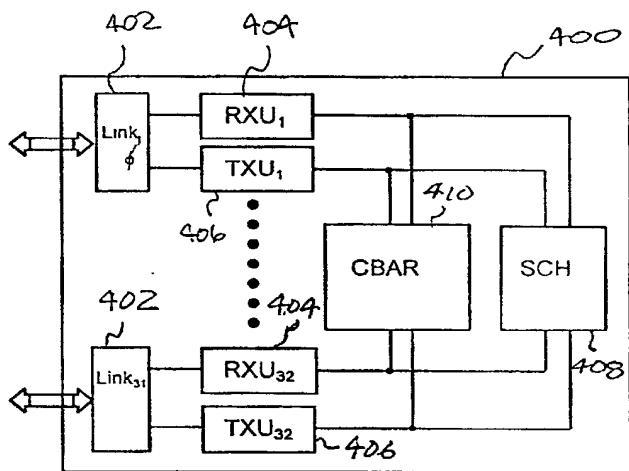


FIG. 4 [CSW]

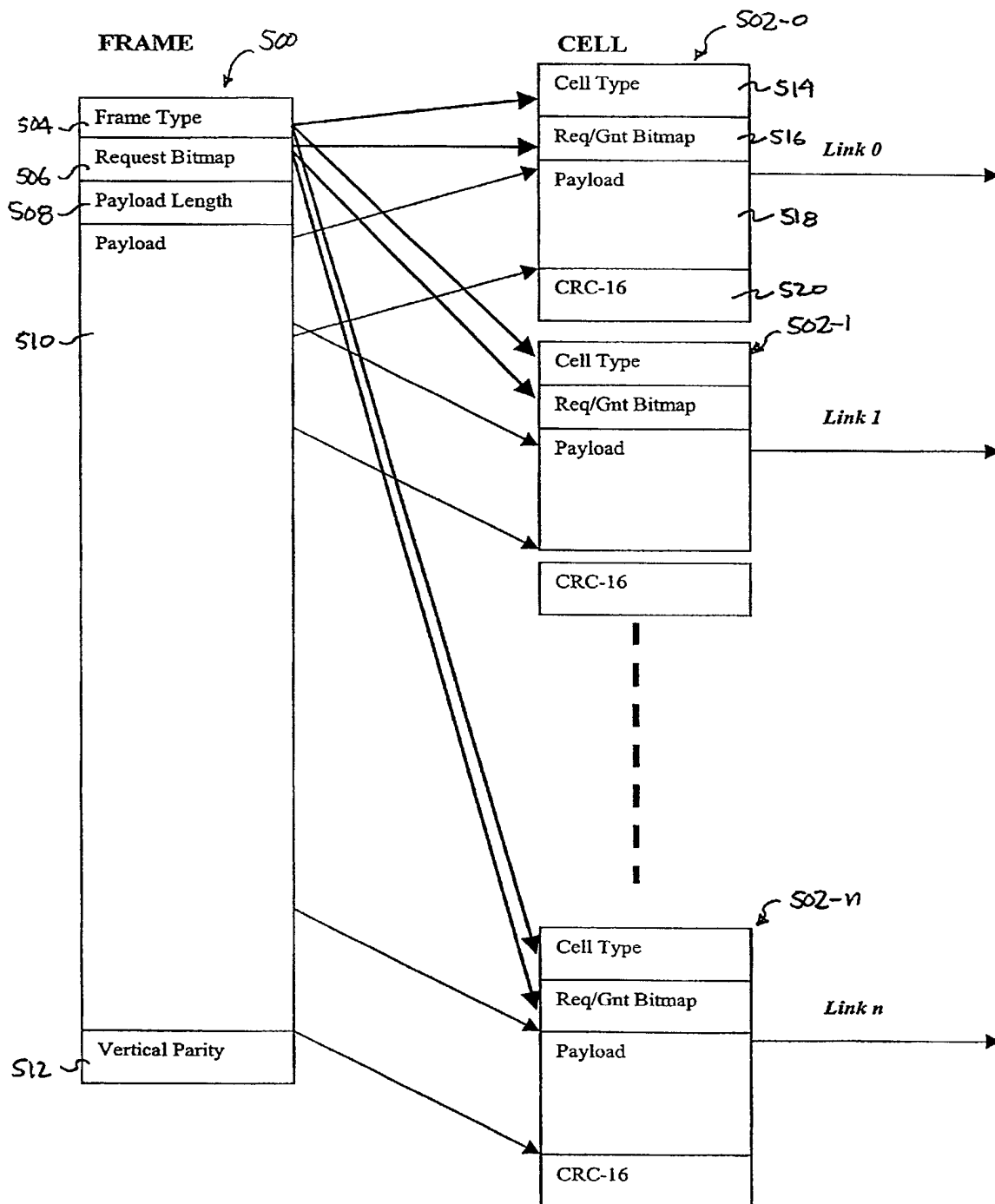


FIG. 5



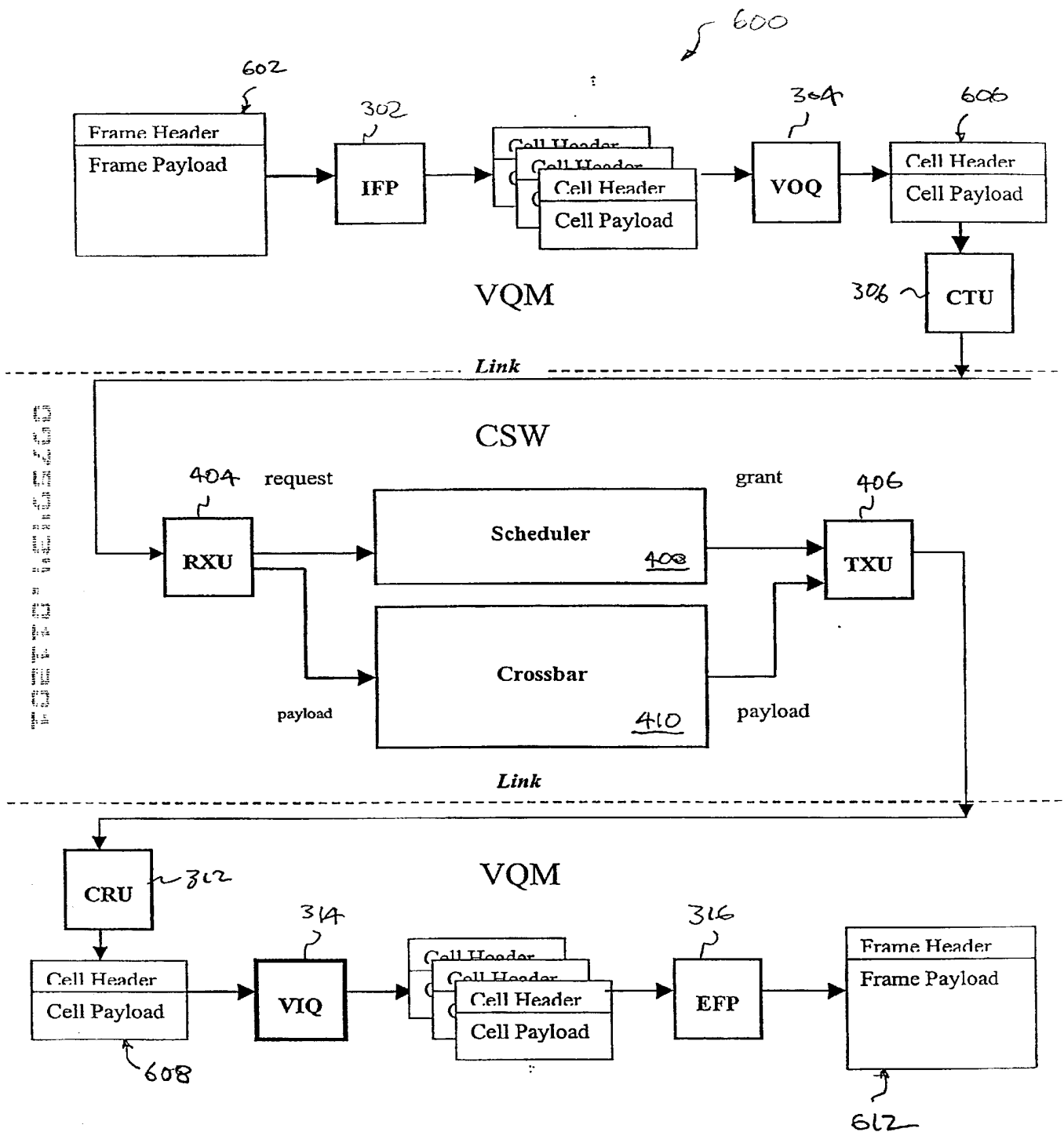


FIG. 6

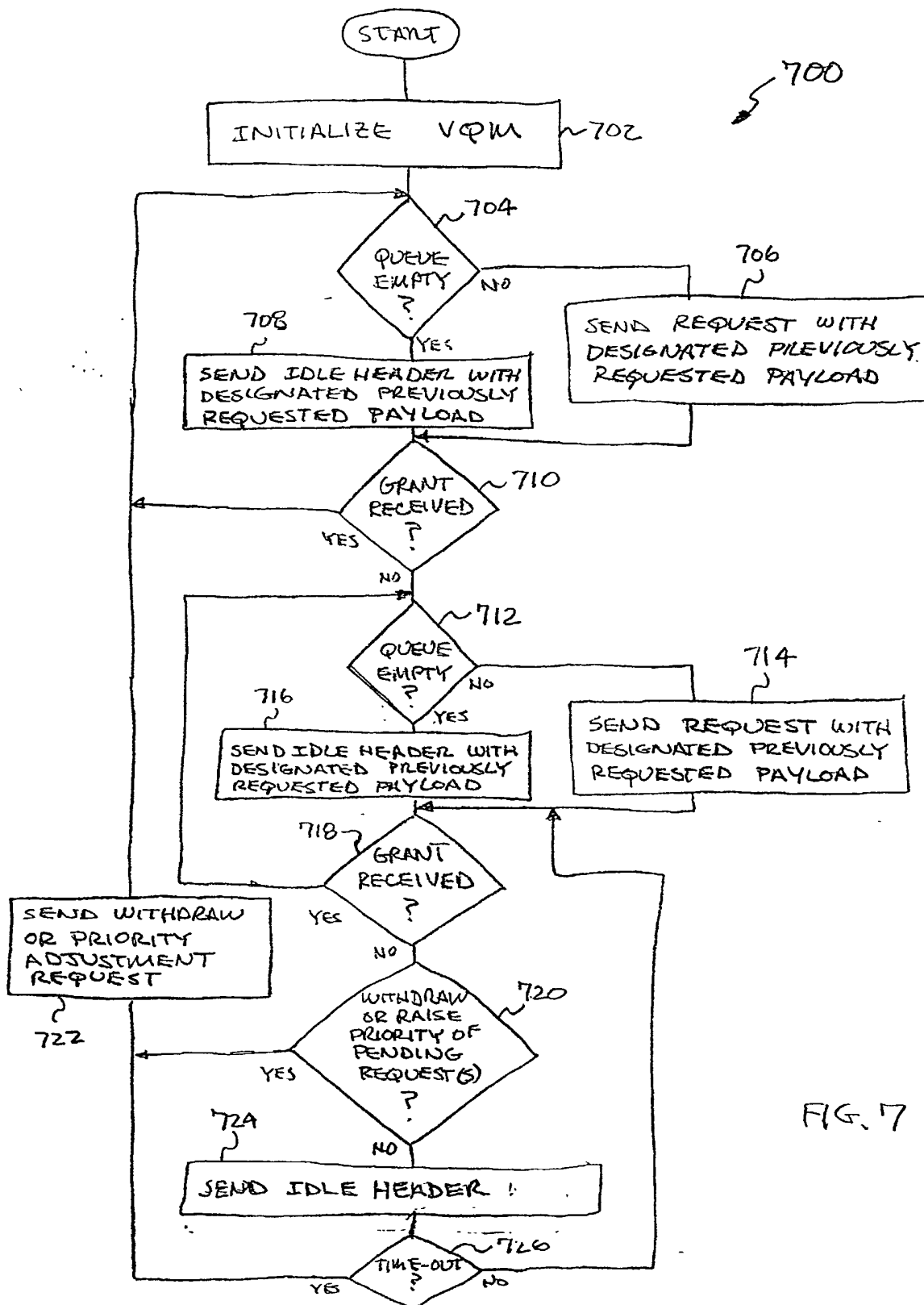


FIG. 7

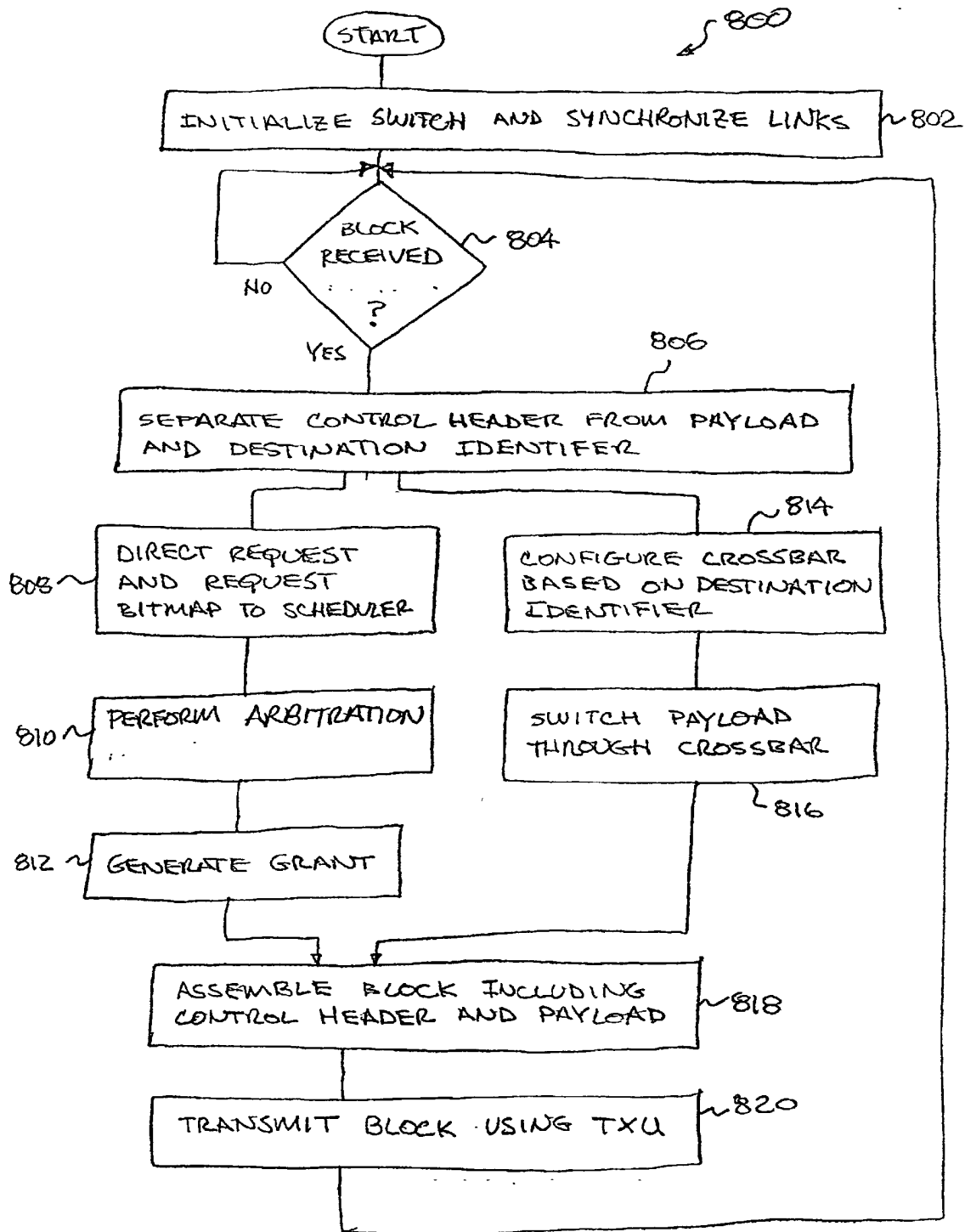


FIG. 8